Bias stress in organic thin-film transistors and logic gates

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Threshold voltage instabilities of all-organic thin-film transistors are investigated as a function of stress time and stress bias. The dominant effect is a positive threshold shift for negative gate bias stress which is explained by mobile ions drifting in the insulator when a gate field is applied. Trapping of charge carriers at the semiconductor–insulator interface plays only a minor role. Furthermore, we investigate the stress behavior of a basic logic element, an inverter. In comparison to a single transistor, we observe improved stability which arises from partial compensation of the parametric shifts during operation. © *2001 American Institute of Physics.*
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All-organic transistor circuits have been proposed for applications such as wireless identification tags, drivers for flexible displays, etc. In the past few years, there has been tremendous progress on the necessary prerequisites such as device fabrication and materials optimization (for a review, see Ref. 1). Studies of the operational lifetime, however, are scarce, and have so far only been performed for hybrid devices comprising an organic semiconductor on an inorganic substrate which incorporates metal electrodes and a SiO_2 insulator layer.[2,3] Negative gate bias stress causes a negative threshold shift, while the mobility remains unchanged. This effect was assigned to the trapping of charges in less mobile states located in the semiconductor, at the interface to the insulator, or in the insulator itself. Similar results were previously obtained on amorphous silicon thin-film transistors (TFTs) and attributed to charge injection into the SiO_2 insulator.[4]

These earlier stress measurements on organic and inorganic amorphous semiconductors exhibit an important similarity in the device structure, namely, a common insulator (SiO_2) which plays a decisive role in the stress behavior, as discussed above. All-organic TFTs which incorporate an organic insulator may show new effects and, as a consequence, different behavior. We have studied TFTs based on the solution-processed semiconductor pentacene (as used in Ref. 2), in which the electrodes were manufactured from polyaniline and the insulator from a commercial photoresist (200 nm layer of SC100, Olin Hunt).[5] Wafers were manufactured on glass substrates which were planarized with a resist layer. The devices had a channel length of $L=2.5$ μm and a width of $W=500$ μm. Stress measurements were performed with an HP4156B semiconductor parameter analyzer. The samples were kept in air and in the dark at room temperature (25 °C). Threshold voltage shifts after application of a constant bias stress were measured in the linear regime, i.e., with the gate voltage being much larger than the voltage between the drain and source $[V_{ds} \ll (V_g - V_T)]$. The threshold voltage V_T was determined from the channel current, which in first order is given by

$$I_{ds} = \frac{W}{L} \mu C (V_g - V_T) V_{ds} . \quad (1)$$

Here, C is the capacitance per unit area of the insulator and V_g the gate voltage. The field-effect mobility μ remains constant during stress, as was previously observed in hybrid pentacene transistors.[2]

In order to obtain insight into the stress behavior, we performed two series of measurements: one in which we kept the drain bias fixed at $V_{ds}=-10$ V while varying the gate bias, and a second one at fixed gate bias ($V_g=-10$ V) with varying drain voltages.

Figure 1 shows the results of the first series. For zero gate bias, we observe only a small shift of the threshold voltage showing that source–drain stress alone has nearly no impact on device characteristics. Upon application of a gate voltage during stress the behavior is at first hardly changed: A slightly negative ΔV_T occurs on short time scales, which is attributed to charge trapping. The effect, however, is much smaller than in hybrid TFTs based on pentacene.[2] On longer time scales, positive threshold shifts are observed, meaning that V_T moves in the direction opposite to that of the applied gate bias. Thus, there is a second effect with a polarity opposite to charge trapping. This positive shift is even more

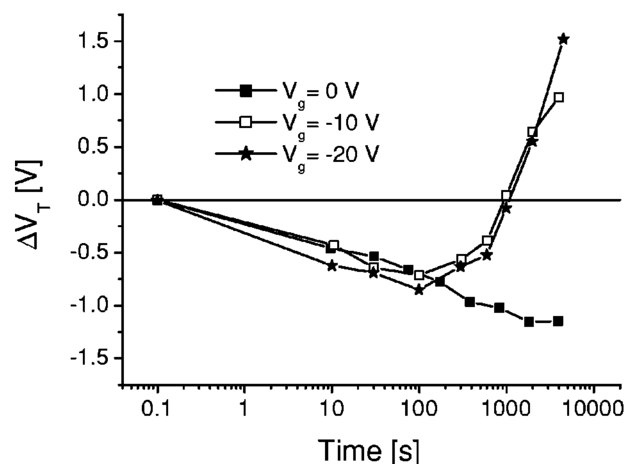

FIG. 1. Threshold voltage shift ΔV_T as a function of time and gate bias V_g at a fixed source drain–source bias of $V_{ds}=-10$ V.

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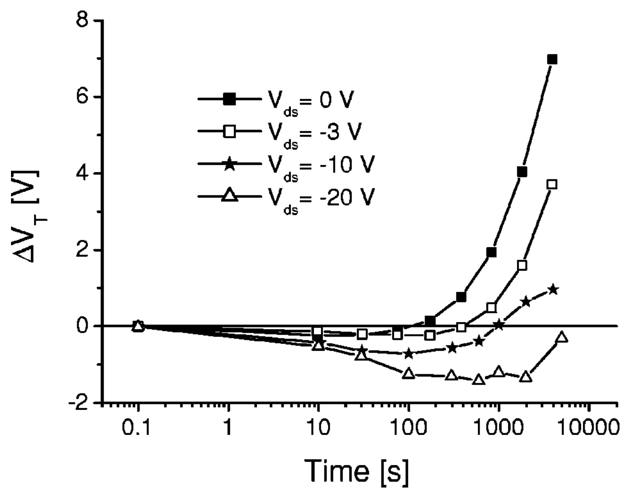

FIG. 2. Threshold voltage shift ΔV_T as a function of time and drain–source bias V_{ds} at a fixed gate bias of $V_g = -10$ V.

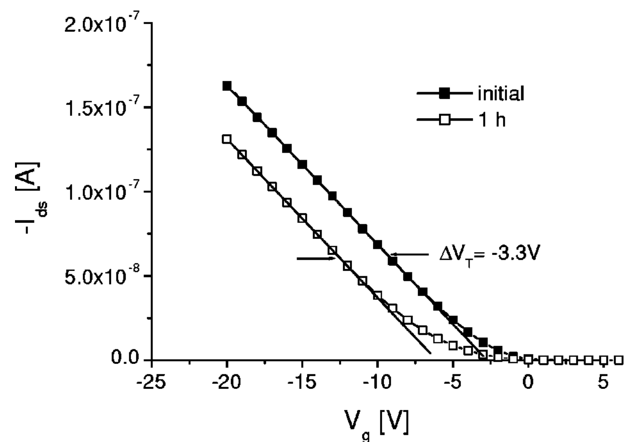

FIG. 3. Gate sweeps of a pentacene TFT measured in vacuum after annealing at 50 °C. The device was stressed for 1 h at $V_g = -10$ V and $V_{ds} = -1$ V. A threshold shift of −3.3 V is observed.

pronounced in Fig. 2 which depicts the threshold voltage shift at fixed $V_g = -10$ V and varying V_{ds}. For $V_{ds} = 0$, a positive shift of up to 8 V is observed after 4000 s (for longer stress times, a saturation of the threshold shift occurs). Its magnitude decreases with increasing V_{ds} because a negative V_{ds} generates an electric field over the insulator which opposes the gate bias. However, the gate bias cannot be completely screened by applying a drain field, since the source contact remains on ground.

A possible explanation for the observed positive threshold shift upon negative gate bias stress can be found in a paper by Young and Gill[6] on polycrystalline Si TFTs formed with undensified insulator oxides. These porous oxides (which contain a significant amount of water) bear more resemblance to an organic insulator than the thermally grown SiO_2 layers used in previous studies on organic hybrids. Young and Gill observed positive threshold shifts arising from negative ions which were moving in the gate field.[6] As the negative ions drift towards the interface to the semiconductor, positive countercharges (holes) accumulate on the semiconductor side of the interface to the insulator. This manifests itself electrically in a positive shift of the threshold voltage. Because the ionic effect vanished after annealing the device to 250 °C, Young and Gill concluded that water absorption in the insulator may be its origin. We have performed measurements with a quartz crystal microbalance and found that the water content of our insulator is 1–2 wt % at relative humidity of 60%. Upon varying the relative humidity, a new equilibrium concentration is achieved within minutes. To eliminate possible water effects, stress measurements were carried out in vacuum (10^{-4} mbar) with samples which were annealed at 50 °C for several hours. Under these conditions, no positive shift is observed, as is depicted in Fig. 3. ΔV_T is purely negative, which is indicative of charge trapping. The influence of water was further confirmed by flooding the chamber with different gases after annealing. Synthetic air which is water free produced similar results as the vacuum measurements, excluding the possible influence of oxygen. Flooding with (wet) room air, however, yielded positive threshold shifts similar to those seen in Fig. 2. These observations demonstrate that water is a necessary prerequisite for positive threshold instabilities.

An important question, however, remains. It is not clear whether the water provides the mobile ions itself (H^+ and OH^-), whether a water network is formed in the insulator, or whether water generates high-mobility paths for already present ionic impurities. These ions may arise from residual ions in the insulator (present at a level of less than 3 ppm)[7] or from doping ions migrating from the polyaniline electrodes. To address this issue, further experiments are in progress.

We also investigated the electrical reversibility of bias stress. Figure 4(a) shows the threshold voltage shift of a transistor which was stressed at $V_g = -10$ V for 1 h (closed boxes). Afterward, the bias was reversed ($V_g = +10$ V, open boxes) for another hour. The initial threshold voltage is al-

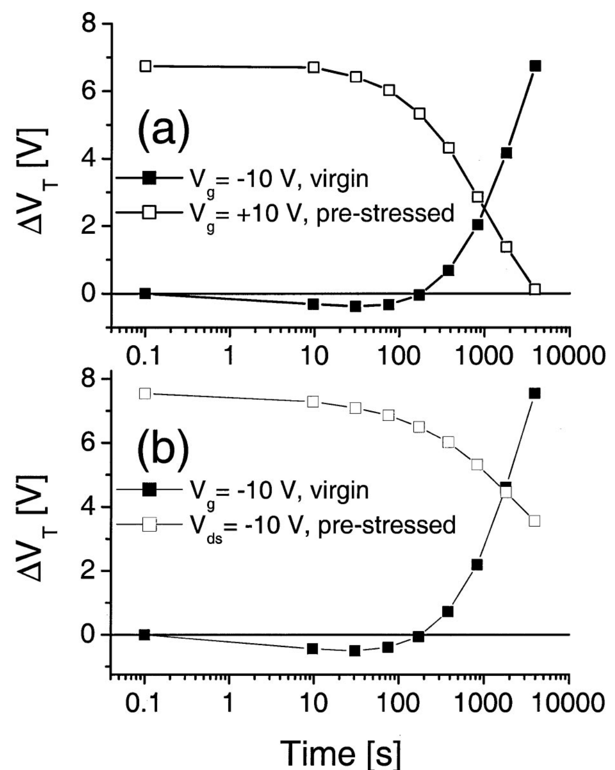

FIG. 4. (a) Threshold voltage shift of a transistor stressed at $V_g = -10$ V (closed boxes). It fully recovers after reverse bias at $V_g = +10$ V (open boxes). (b) A transistor stressed at $V_g = -10$ V (closed boxes) partially recovers after being stressed at $V_{ds} = -10$ V (open boxes) for the same time.

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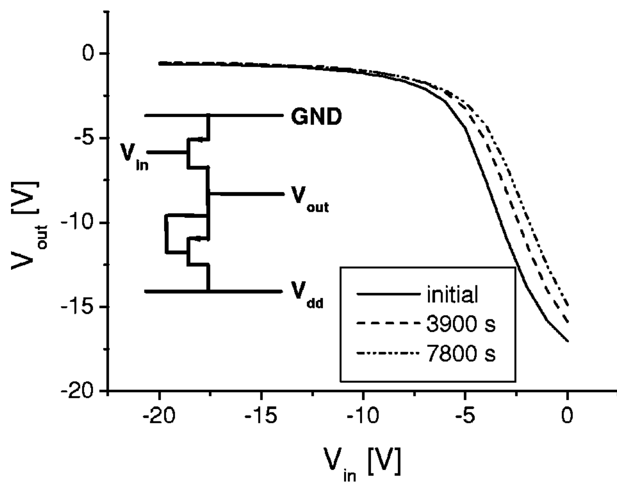

FIG. 5. Transfer characteristics of a stressed inverter as a function of stress time. Inset: Schematic of the inverter.

most recovered. Figure 4(b) shows the result of a second experiment, where, after similar initial stress on another transistor, pure drain stress was applied for 1 h ($V_{ds} = -10$ V, gate grounded). The threshold shift is greatly reduced, however the initial situation is not restored. A negative V_{ds} generates a gate field of the same direction as positive V_g, however the field will be inhomogeneous, since the source remains grounded. Thus, complete recovery cannot be expected. One can also argue that charge trapping—causing negative threshold shifts—may play a role in device recovery. However, a comparison with Fig. 1 shows that source–drain stress of the same magnitude leads to much smaller shifts on a virgin device, namely -1.2 V as compared to about -4.2 V on the prestressed sample.

Having studied threshold voltage shifts and their reversibility on a transistor level, it is interesting to make a connection to logic circuits and wonder about their stability under bias stress. Our current circuit design[5] is based on inverters (for a schematic, see the inset of Fig. 5) and *NAND* gates. An inverter can be in two stable states during operation, and is defined by the input voltage V_{in} being low (equal to the circuit drive voltage V_{dd}), or high (V_{in} grounded), respectively. The load transistor which is the lower device in the schematic has in both states the gate connected to the source, whereas V_{ds} changes approximately between V_{dd} and zero. Therefore, the load transistor is only subject to pure drain stress which was shown to cause little change of V_T (see Fig. 1).

Consequently, the parametric instability of an inverter is determined by the input transistor. When V_{in} is low, its V_{ds} is close to zero, and the gate voltage is equal to V_{dd}. Then, the input transistor is subject to pure gate stress. When V_{in} is high, its gate is grounded. At the same time $V_{ds} \approx V_{dd}$, which corresponds to pure drain stress. Consequently, the input transistor alternates between pure gate and pure drain stress. Similar to Fig. 4, drain stress generates an opposite, but inhomogeneous, gate field, thus reducing the influence of gate stressing. The net result is improved parametric stability of the inverter, as depicted in Fig. 5.

Our measurements demonstrate that bias stress in all-organic TFTs manifests itself predominantly in the form of a positive threshold voltage shift for negative gate bias stress. This instability arises from the movement of ions in the gate field and is connected to the water that is present in our devices. Charge carrier trapping, which would yield negative threshold shifts, plays only a minor role. Furthermore, bias stress has no influence on the mobility. Future studies will be aimed at clarifying the nature of the ionic species involved as well as the influence of bias stressing on the subthreshold behavior. Logic based on inverters shows operational stability that exceeds that of individual transistors due to partial compensation of the parametric instabilities during inverter operation.

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